Status of FE Electronics for ATLAS Pixels

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Summary of previous results

- Two major rad-soft electronics designs, with many lab and testbeam results.
- System design and many details of FE design validated.

Results from recent DMILL FE run

- Recently received wafers from DMILL engineering run
- Summarize current knowledge of chip operation.

Next steps:

- Re-submission of FE-D engineering run
- Submission of Honeywell SOI FE-H engineering run

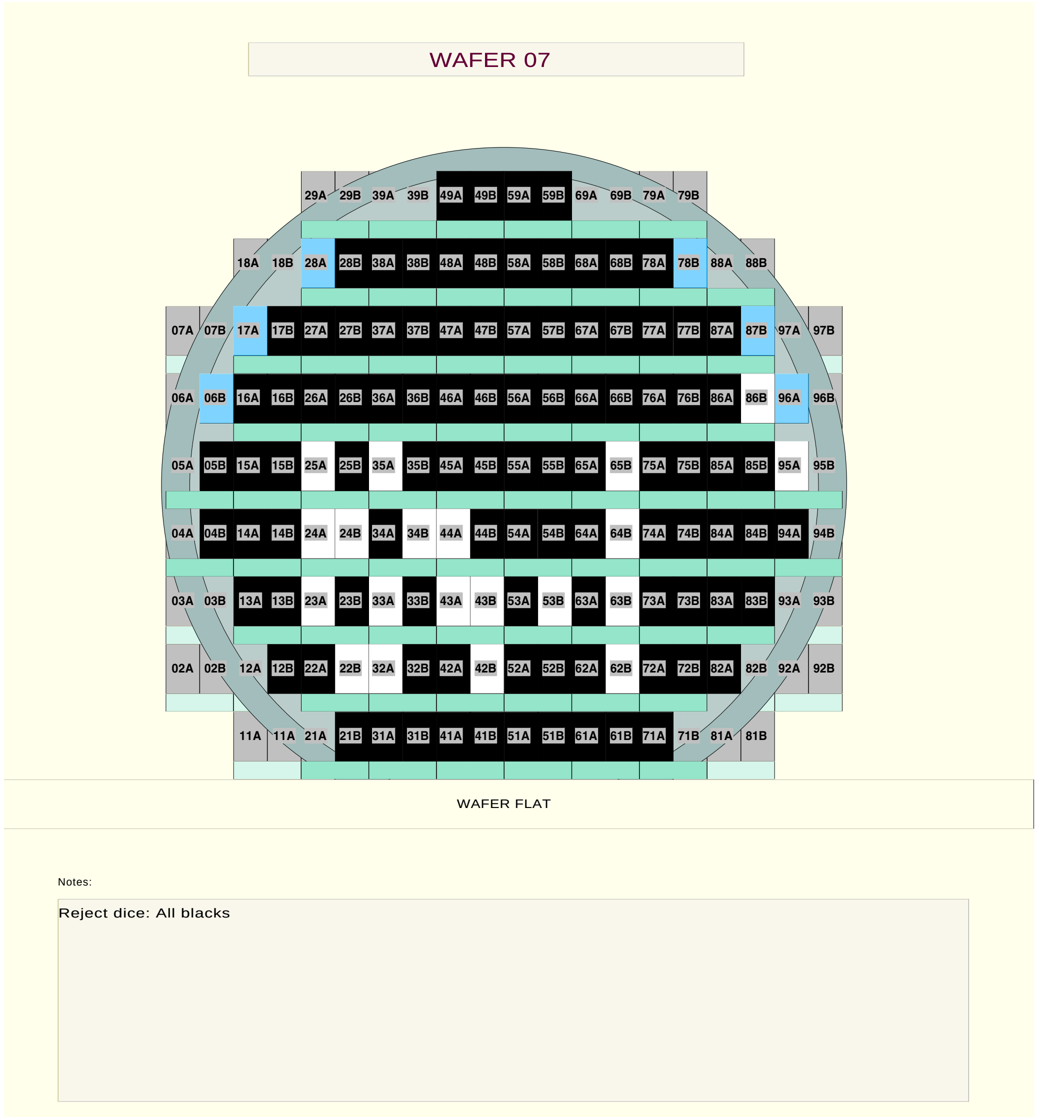
Summary of Previous Results

- Prototyped complete system design ("Demonstrator Program") for the Pixel on-detector electronics, using rad-soft commercial processes during 97 and 98.
- This program included two FE chips (FE-A/FE-C in AMS 0.8µ, and FE-B in HP 0.8µ), and a module controller chip (MCC in AMS). The processes used were chosen to allow natural conversion to TEMIC/DMILL and Honeywell/SOI rad-hard processes.
- The FE chips used our final geometry (7.4x11.0mm die size and 7.2x8.0mm active area) with 2880 pixels of size 50µ x 400µ, and included almost all essential circuit blocks. They were both about 800K transistor chips, with all full-custom layout. The MCC was a 400K transistor chip which was largely synthesized using a "silicon compiler".
- There were a number of minor errors in all of the chips, but they all worked well enough to carry out major prototyping programs over the last 2 years in our labs and the H8 testbeam. Single chips with a variety of sensor designs, including irradiated sensors, were tested in 98. In 99, the emphasis shifted to complete 16-chip modules, including the MCC.
- This results confirmed the basic designs and lead us to the rad-hard generation of prototype chips, design of which was started in July 98. We are pursuing a two-vendor program, first using DMILL and then using HSOI.

Overview of DMILL FE Development

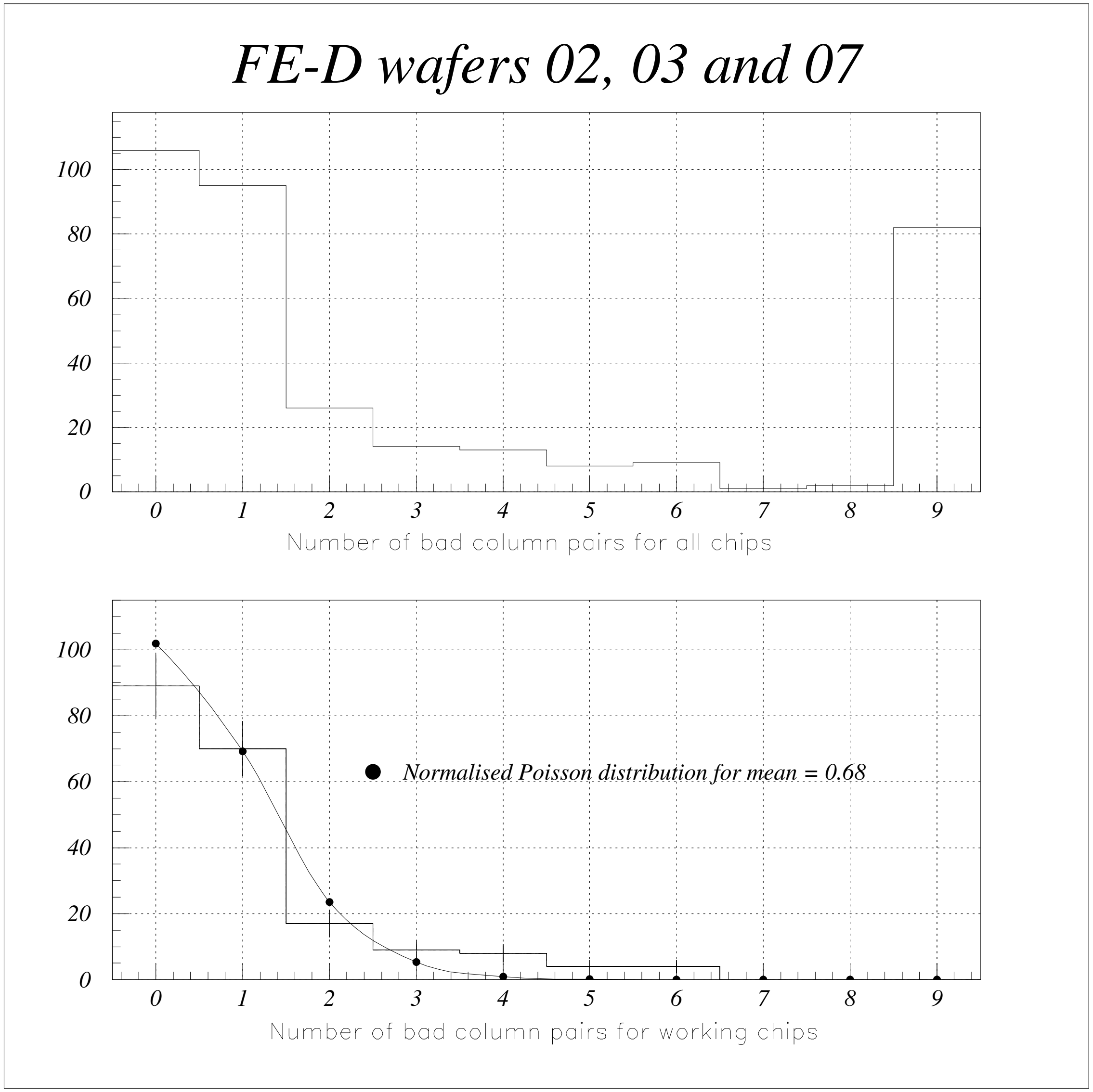
- Began common design in July 98. This work included FE-D (front-end chip), a prototype MCC containing many elements of a final design (MCC-D0), opto-link chips in DMILL (DORICp and VDCp), as well as several additional test chips.
- The complete reticle was submitted on Aug. 10 this year, and first wafers returned to CERN at the end of October (we paid acceleration fee to TEMIC).
- First results on FE-D emerged from wafer probing, and indicated several problems. These included a layout error between two capacitors, which should have been detected by TEMIC LVS/DRC, and which killed a circuit block generating an internal threshold control voltage. This problem can be by-passed using FIB surgery.
- Additional problems were found in the digital circuitry, including some buffering problems in the command decoder (software workarounds possible), as well as a clock distribution problem. The implications of the clock distribution problem are still being studied.
- All basic chip functions verified, including many aspects of analog performance. Still some concerns about performance in the front-end, including threshold dispersion and timewalk. Further studies needed.
- Two serious problems observed with chips. First is yield, and second is operating voltage for digital circuitry. The latter may be largely caused by clock distribution.

Wafer Maps



- Results of wafer probe of one wafer using simple digital tests. These include correct operation of Global Register (100 bit control register at bottom of chip) and Pixel Register (2880 bit control register in matrix), and ability to correctly transmit event data.
- Three wafers probed so far, and yield for these tests is only about 25%.
- More sophisticated tests have even lower yield. In particular, no chip has anything close to zero dead channels for digital tests (previous HP chip had 92% yield for such tests).

- Have analyzed the Pixel Register problem in more detail, using column-masking to divide register into 9 column-pairs, and studying bad column pair rate:



Look at distribution of number of bad column pairs in register per die.

Remove chips that are already bad for other reasons.

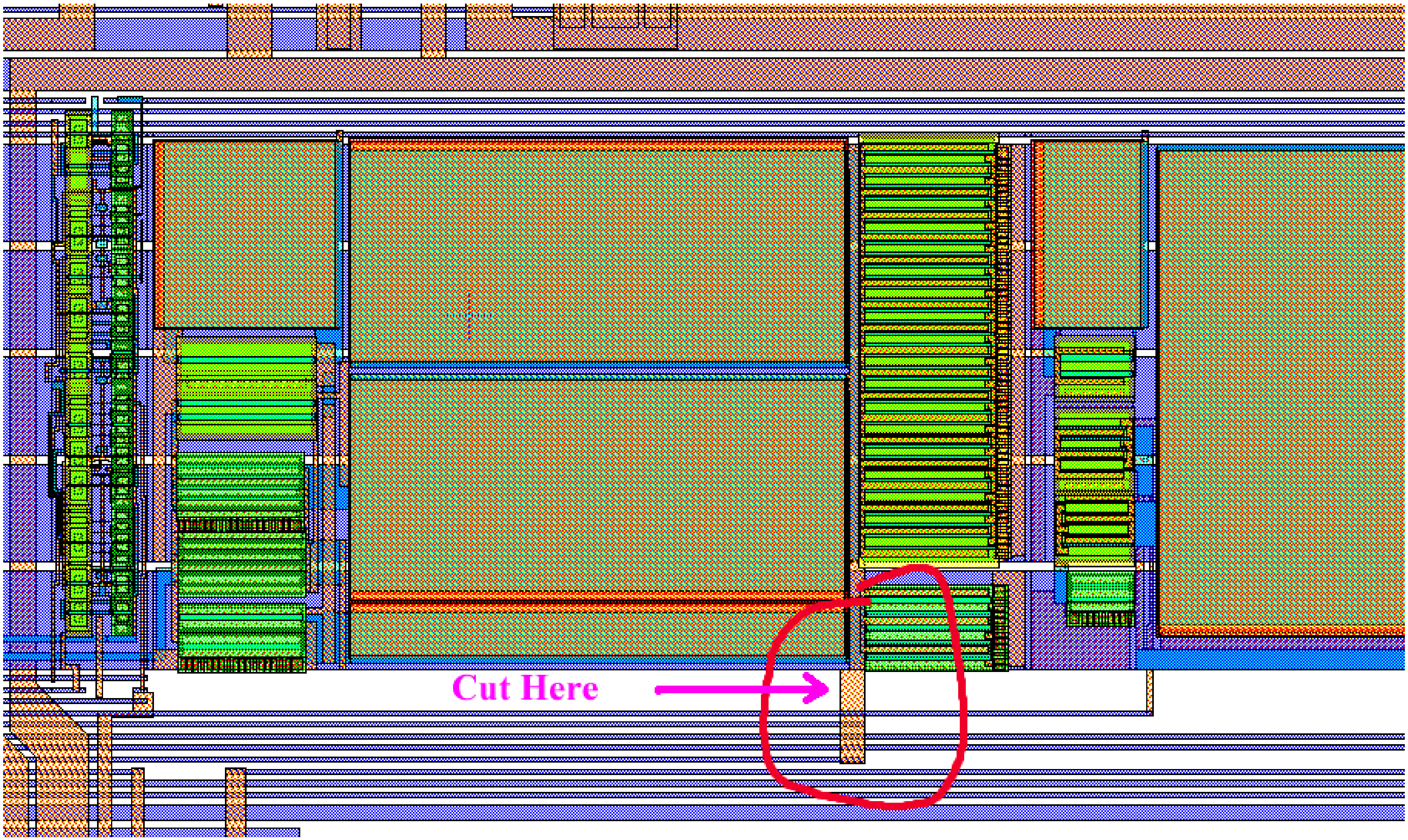
Find well-described by Poisson, with mean of 0.6.

This confirms notion of single-point defects, but with a very high defect density (shift register area about $4mm^2$).

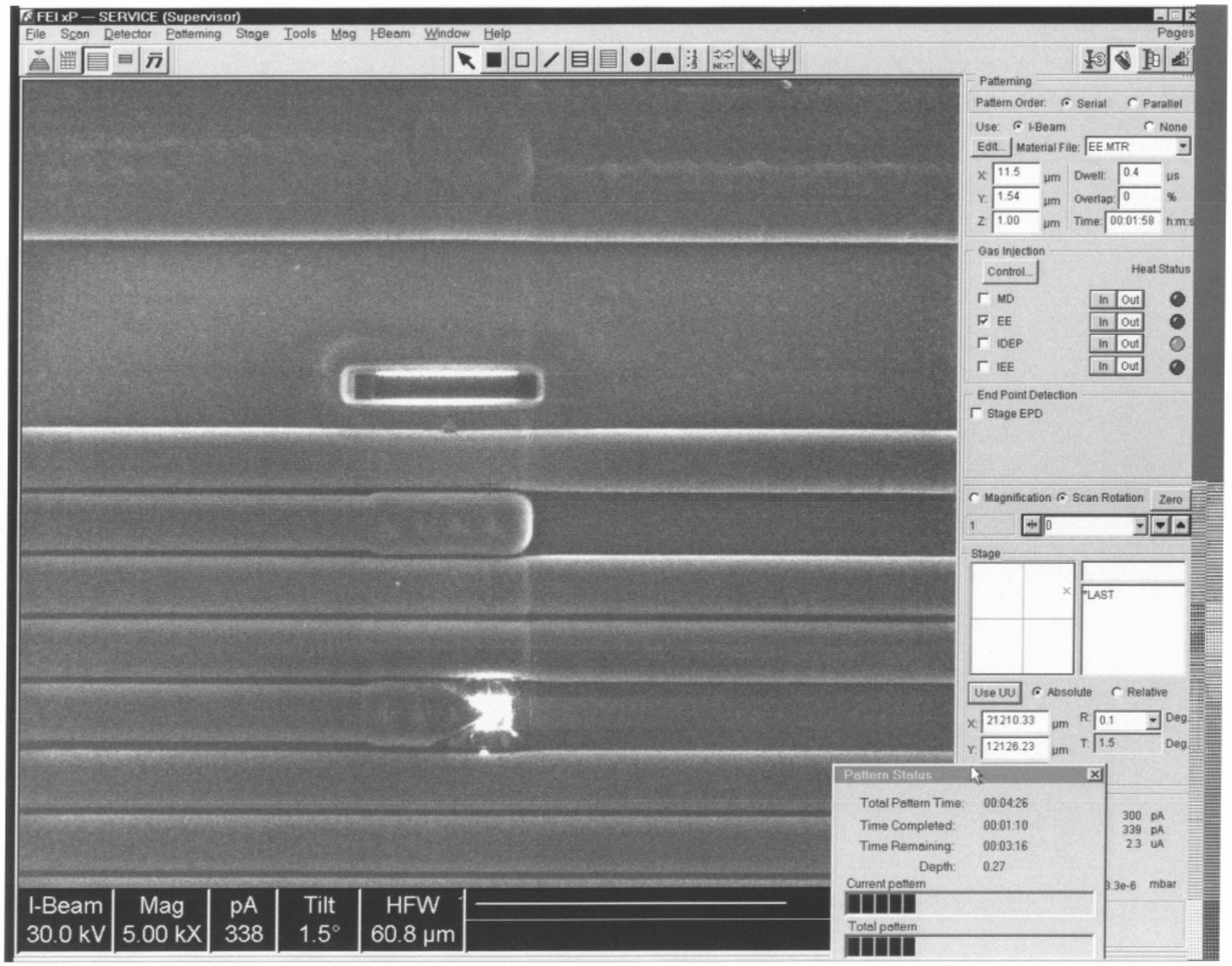
Suspect yield arises from high off-current in NMOS used in dynamic FF. This requires about 1 out of 1000 NMOS to fail in this way, but static logic should not be affected.

FIB Modification of Wafer #7

- Decided to completely dice the lower half of wafer #7, and to perform FIB modification on 15 die with 9 good column pairs in Pixel Register test in order to allow external supply of VTH for front-ends.



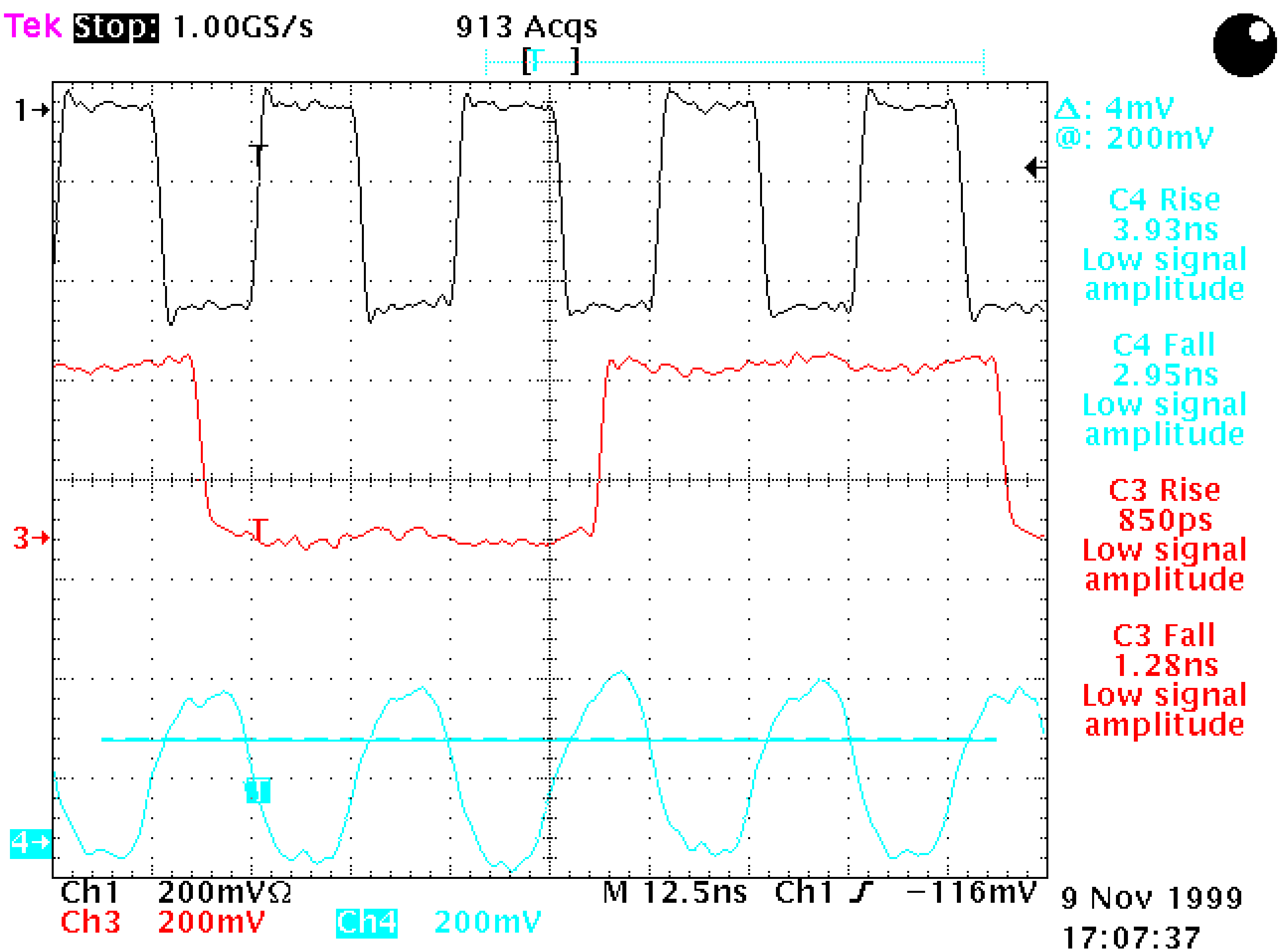
- Modification of each die took about 8 minutes on FIB machine at Accurel:



- Cut of approximately 11µ length was made through 9µ wide M1 trace.
- Under SEM, can see the Al remnants of the original trace as bright lines.

Measurements of Digital Readout Circuitry

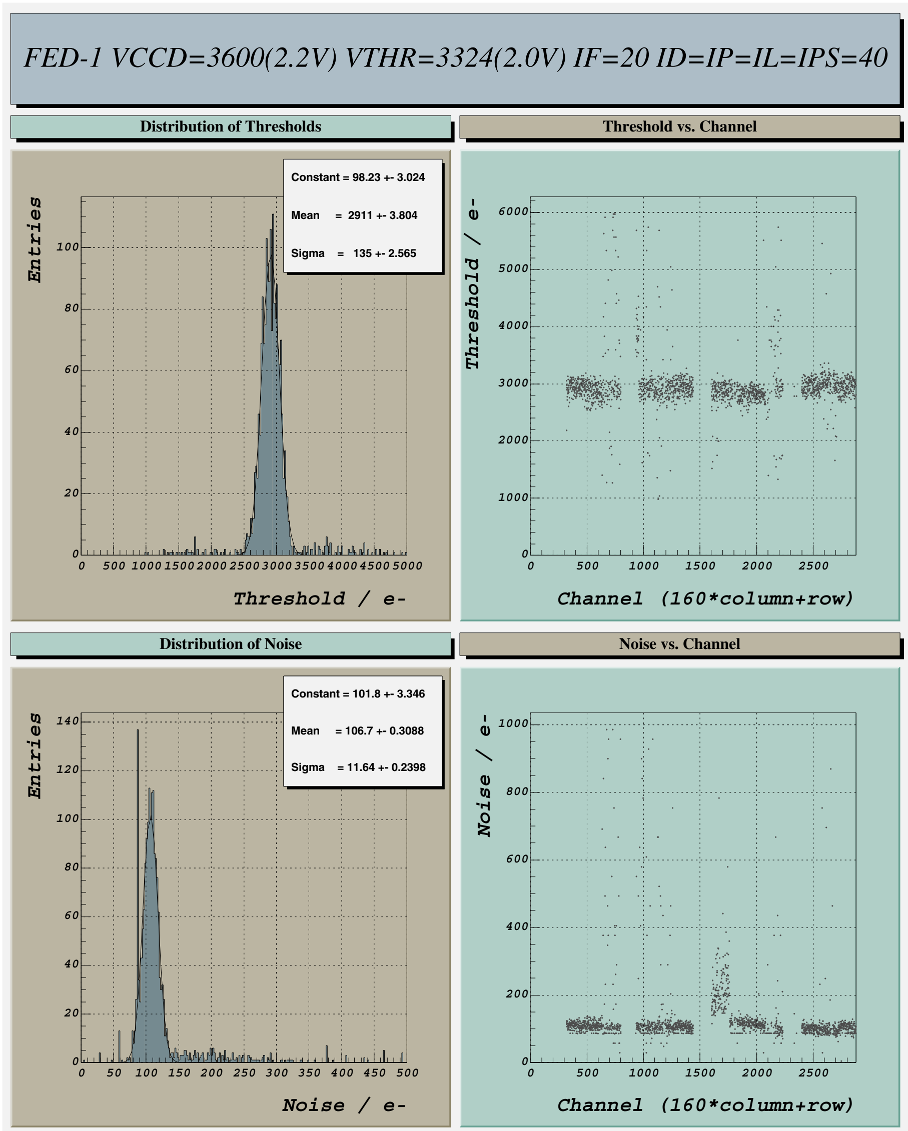
- Realized that there is a serious problem with XCK distribution inside FE-D, with relatively small transistors in LVDS receiver driving a fanout to 72 FF over a large, minimum width, set of busses.



- Observe very poor risetime on internal XCK of about 5ns (10-90%). Duty cycle at VDD/2 is still 50%.
- For reference, TSC0 is also shown. It has a risetime of about 1ns, as expected for the combined Picoprobe and scope bandwidth (500 MHz).

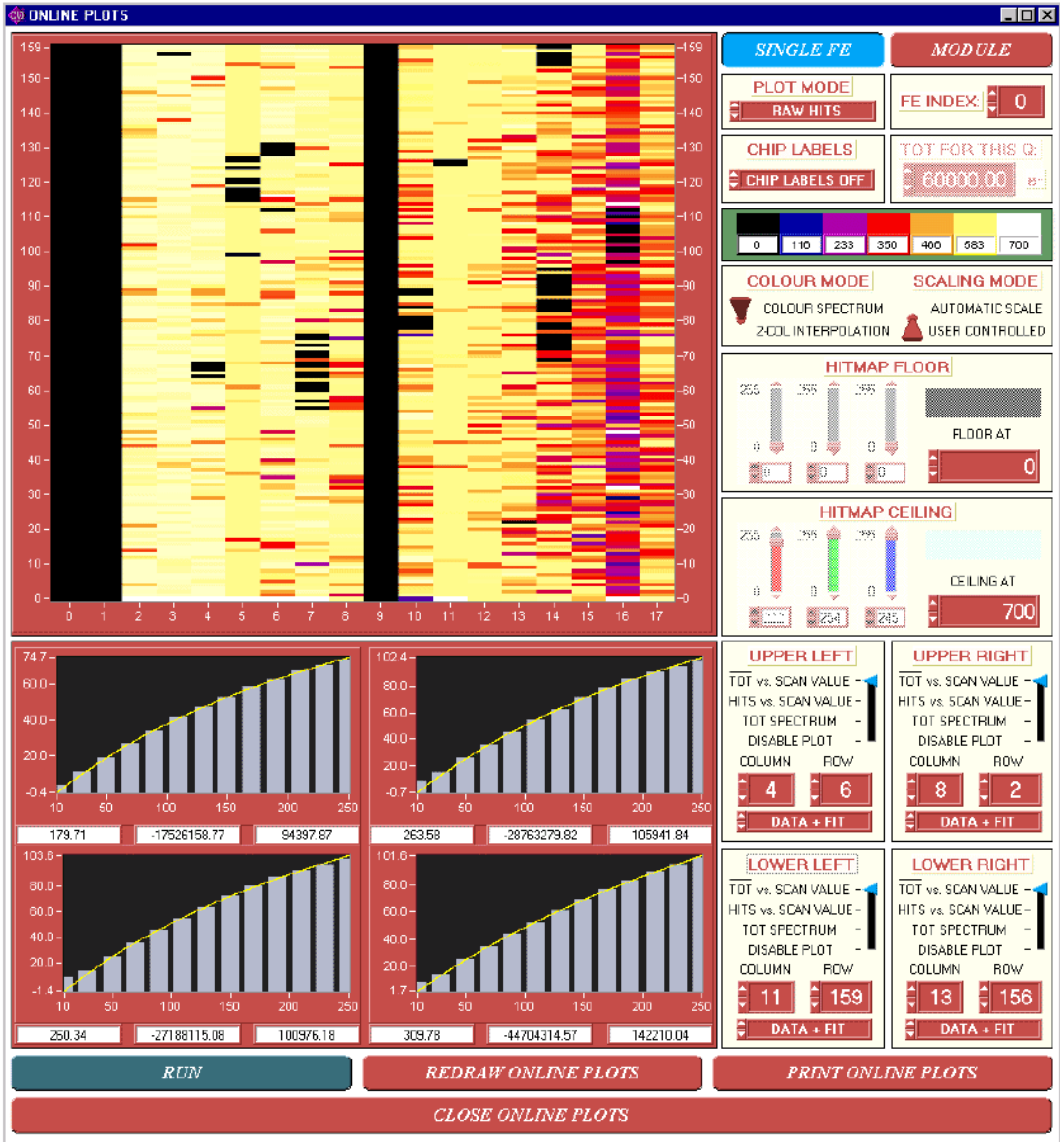
Examples of Analog Scans

- After tuning, see expected improvement in threshold dispersion:



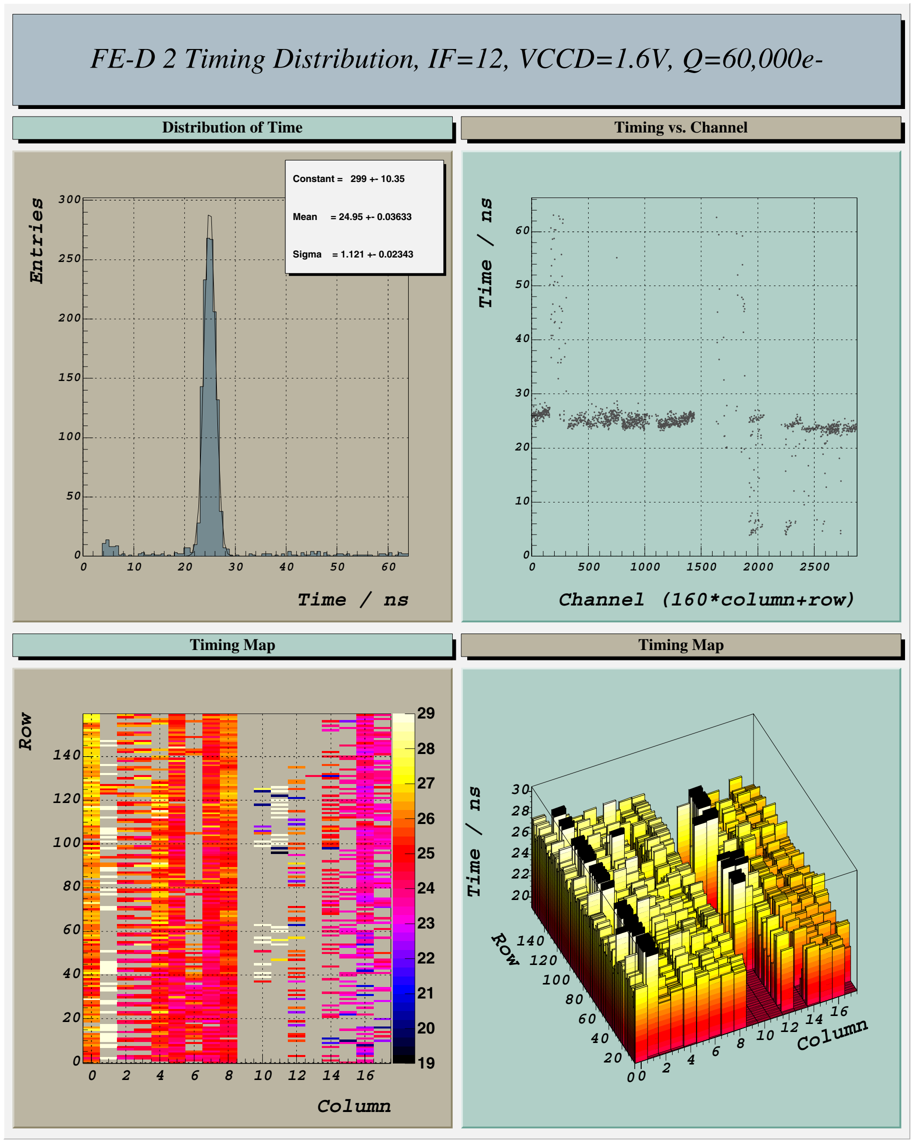
- After tuning, the dispersion is reduced to about 135e.
- The noise is about the same, but this particular chip shows fluctuations in the noise behavior, and is often much noisier.

- Do a TOT scan as well to look at dispersion (required increasing IF from 20 to 35 to avoid loosing hits with large charge). Used FE-D #1:



- TOT response curve is quite nice at high VCCD.
- Units are DAC counts for internal chopper DAC.

- Have also performed timing studies by injecting a large charge (60Ke) and scanning the delay to find when the hit moves from one crossing to the next:



- Scan was done for FE-D #2
- Perhaps some small indications of systematic effects, but chip had many bad/dead channels, so it is hard to tell.
- Taking an RMS over the channels gives 1.1ns, which is similar to the results obtained from FE-B in the past.

Summary of FE-D and Next Steps

Overall comments:

- FE-D requires very high VDD voltage to operate properly (far beyond anything which is acceptable). Limiting factor seems to be data corruption, possibly related to XCK of serializer, or relative timing of serializer and output MUX (speculation). Difficult question is to what extent this is a result of problem with XCK distribution, and to what extent it is a separate problem.
- There is a very significant yield problem. In the first wafer, only 19% of the die pass minimal digital tests. It seems very unlikely that this is a design problem on our part. The yield problem also appears as a large number of local fabrication defects in each die. Of the chips examined in detail, all have many ten's of individual bad channels, as well as bad column pairs, noisy column pairs, etc. None are close to a chip we could use in an ATLAS module.
- We cannot evaluate TEMIC as a vendor for pixels based on the performance of this chip. We will work over the next few months to fix all problems that we can find, and re-submit the chip in a new engineering run. We will meet with TEMIC in Jan. 00 to discuss our results and possible improvements for the next run.
- This will mean significant delay for the pixel "module 0" program.

Other Results from FE-D Run

- MCC-D0 tested, and appears to be working. The command decoder and the prototype FIFO are OK, but the FIFO is not testable at full speed. Note that this is completely incompatible with the defect density observed in FE-D if we assume the defects are “generic” and affect all types of circuitry in the same way.
- DORICp tested in preliminary way. Appears to work properly at 5V (it decodes command data and 40MHz clock), but not at 4V (locks to 20MHz). Internal nodes are available for debugging with probes.
- Analog test chip extensively studied, and many nice results on FE-D front-end have been measured.
- Will extract device parameters from PM bar (includes L/W arrays and example devices from front-end). Some indications that the preamp risetime is worse than expected (as well as timewalk), so want to confirm PMOS g_m in particular.
- Propose that analog test chips are irradiated, along with PM bars containing analog devices used in front-end.
- LVDS buffer will be tested this week using new rad-hard FE-D testboard. This is our vehicle for irradiating FE-D chips while they are operating.

Status of FE-H Design

- TAA agreements now essentially in place with all European design groups.
- Some design goals are more ambitious for this process, since density and rad-hardness appear better than for DMILL. This includes targeting design for B-layer, including 300μ pixels, and increased buffering in EOC for higher occupancy.
- Design work for digital readout has been proceeding for several months. It looks as though time can be saved by developing a standard cell library and synthesizing some blocks in the chip.
- Design work just beginning for front-end conversion from DMILL. Expect this to take about 4 months of work.
- Intend to complete chip for submission in about May 00, but our design community is severely strained by the need to iterate on FE-D chip in the same period.
- Critical paths for the submission are likely to be the front-end design, plus the EOC and BOC region where lots of hand-crafted layout work is required.